BUI THANH DAT

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Education

- **Clemson University** *Expected Start: Aug 2026*
  Incoming Ph.D. Student in Computer Science (Fully Funded) South Carolina, USA
  - Advisor: Dr. Zhenkai Zhang
  - Awarded a full Graduate Research Assistantship (GRA), providing full tuition coverage and a living stipend.

- **University of Science, VNUHCM** *2021 - 2025*
  Bachelor of Science in Electronics and Telecommunications Engineering Ho Chi Minh City, Vietnam
  - GPA: 8.72 / 10.0 (3.7 / 4.0)

Publications

[C.1] Nguyen, NH., Dang, TP., **Bui, TD.**, Hoang, TT., Pham, CK., Huynh, HT. (2024). Designing and Implementing a 2D Integer DCT Hardware Accelerator Fully Compatible with Versatile Video Coding. In: Gervasi, O., Murgante, B., Garau, C., Taniar, D., C. Rocha, A.M.A., Faginas Lago, M.N. (eds) Computational Science and Its Applications - ICCSA 2024 Workshops. ICCSA 2024. Lecture Notes in Computer Science, vol 14815. Springer, Cham. https://doi.org/10.1007/978-3-031-65154-0_7

[C.2] Nguyen, NH., Dang, TP., Tran, TK., **Bui, TD.**, Hoang, TT. and Huynh, HT., "A Configurable 2D-Integer DCT Hardware Accelerator Compatible with H.266 Standard based on RISC-V Architecture," 2024 7th International Seminar on Research of Information Technology and Intelligent Systems (ISRITI), Yogyakarta, Indonesia, 2024, pp. 894-899, doi: 10.1109/ISRITI64779.2024.10963564.

[C.3] Huynh, TMT., Tran, TK., **Bui, TD.**, Pham, CK., and Huynh, HT. (2025). An Efficient Algorithm Compatible with Low-performance Hardware for AI Edge Devices in Arrhythmia Prediction. In: Proceedings of the Fifth International Conference on Intelligent Systems and Networks. Singapore: Springer Nature Singapore, 2026, pp. 254-264. isbn: 978-981-95-1746-6. doi: 10.1007/978-981-95-1746-6_28.

[C.4] Pham, DH., Huynh, TMT., Tran, TK., **Bui, TD.**, Pham, CK., and Huynh, HT. (2025). Efficient AI Model and Hardware Architecture Based on CNN for Arrhythmia Prediction. 2025 10th IEEE International Conference on Integrated Circuits, Design, and Verification (ICDV), Ho Chi Minh City, Vietnam, 2025, pp. 25-30, doi: 10.1109/ICDV66179.2025.11135186.

Research Experience

- **Pre-Doctoral Independent Study & Research Preparation** *Aug 2025 - Present*
  Independent Researcher Remote
  - Advisor & Principal Investigator: Prof. Zhenkai Zhang (Clemson University, zhenkai@clemson.edu)
  - Conducting advanced independent study focusing on computer architecture, memory consistency, and cache coherence to build a foundation for doctoral systems research.
  - Analyzing hardware security vulnerabilities and memory architecture optimizations, evaluating methodologies in papers such as *INVALIDATE+COMPARE* and *GPU Memory Exploitation for Fun and Profit*.
  - Engaging in CPSC 9500 doctoral seminars to integrate with ongoing laboratory research prior to formal enrollment.

- **Remote Collaboration** *2023 - Present*
  Undergraduate Research Student
  - Advisor: Prof. Tung Kieu (Aalborg University, tungkvt@cs.aau.dk)
  - Investigated unsupervised black-box adversarial attacks against Deep One-Class Classification models, specifically within the time-series domain.
  - Explored the use of unsupervised meta-learning for generating effective and transferable adversarial examples.

- Developed understanding of deep learning frameworks, attack methodologies (FGSM, PGD), and model robustness techniques.

- **Computer Embedded Systems Laboratory (CESLAB), HCMUS - VNUHCM** *2022 - 2025*
  Undergraduate Research Student
  - Advisor: Dr. Huu Thuan Huynh (Head of Computer Embedded Systems Department, HCMUS, hhthuan@hcmus.edu.vn)
  - Contributed to the design, implementation (Verilog), and FPGA verification of hardware accelerators and SoC components. Developed proficiency in digital design methodologies, simulation, hardware debugging, and system integration.
  - Conducted a comprehensive study of the RISC-V ecosystem by designing, implementing, and evaluating a Linux-capable System-on-Chip (SoC) with a tightly-coupled Deep Neural Network (DNN) accelerator.
  - Successfully prototyped the complete open-source system on a Xilinx VC707 FPGA, validating the Chipyard framework for complex RISC-V designs and achieving an immense performance speedup compared to software-only implementations.
  - Designed, integrated and tested custom peripherals, including a DMA controller with Avalon-MM interfaces, into Nios V based SoC systems using Platform Designer.
  - Gained practical experience with embedded platforms (STM32, Raspberry Pi, Silicon Labs EFR32 Gecko) and development tools.

PROJECTS

- **Open-Source RISC-V SoC Implementation with DNN Acceleration: A Chipyard Framework Study with FPGA Prototyping** *Apr 2025 - Aug 2025*
  Undergraduate Thesis Project, CESLAB
  - Designed, implemented, and verified a complete Linux-capable RISC-V System-on-Chip (SoC) on a Xilinx VC707 FPGA using the Chipyard framework.
  - Integrated a custom Gemmini DNN accelerator via the RoCC interface, achieving a 1,300x performance speedup on optimized deep learning workloads compared to a software-only approach.
  - Managed a full-stack workflow from high-level Chisel/Scala hardware generation to successfully booting a full Debian Linux operating system on the prototyped hardware.

- **Design and Integration of a Custom DMA Controller on FPGA in a Nios V/m SoC System** *Jan 2025 - Apr 2025*
  Internship Project & Report, CESLAB
  - Designed a custom Direct Memory Access (DMA) controller with Avalon-MM Master (Read/Write) and Slave (Control/Status) interfaces using Verilog.
  - Integrated the DMA controller into a Nios V/m based System-on-Chip using Intel Platform Designer.
  - Implemented and tested the complete system on an Intel DE10-Standard FPGA board.
  - Developed C code application using Ashling RiscFree IDE to configure the DMA, initiate transfers between on-chip memory blocks, and verify data integrity.
  - Documented the design, implementation, and testing process in a formal internship report.

- **Smart Temperature & Humidity Monitoring System with BLE & LCD** *Sep 2024 - Dec 2024*
  Group Project (Course: Computer Interfaces and Data Acquisition)
  - Developed an embedded system on a Silicon Labs EFR32 Blue Gecko board (using Simplicity Studio IDE) to monitor environmental conditions.
  - Interfaced with a DHT11 sensor using GPIO to acquire temperature and humidity readings.
  - Implemented custom Bluetooth Low Energy (BLE) advertising packets to broadcast sensor data wirelessly.
  - Assisted in utilisation and adaptation of Silicon Labs Graphics Library (GLIB/DMD) to display real-time sensor data and system status on a Sharp Memory LCD.
  - Enabled UART communication for user configuration of sensor sampling and BLE advertising intervals.
  - Assisted in programming system logic, sensor interfacing, BLE communication, and display drivers in C.

- **IoT Heart Rate & SpO2 Monitoring System** *Oct 2024 - Dec 2024*
  Group Project (Course: Biomedical Electronics)
  - Developed an IoT system to measure and monitor heart rate and SpO2 levels using STM32 and ESP32 microcontrollers.

- Established UART communication between STM32 and ESP32 for transferring processed sensor data, utilizing custom frame parsing with header detection and CRC checks for reliability.
- Programmed the ESP32 (using Arduino C++) to receive data from STM32 and transmit it to a cloud platform (ThingsBoard hosted on AWS EC2) via MQTT protocol over Wi-Fi.
- Configured an AWS EC2 instance and deployed ThingsBoard for data visualization and dashboard creation.
- Gained experience with sensor interfacing (I2C), inter-MCU communication (UART), IoT protocols (MQTT), cloud platforms (AWS EC2, ThingsBoard), and embedded C/C++ programming.

- **Ported Adafruit Fingerprint Sensor Library from Arduino to C++ for STM32** *Mar 2021 - Apr 2021*
  Microprocessor Course Final Project
  - Role: Lead Developer
  - Successfully adapted and implemented the sensor library for an STM32 embedded board, demonstrating C++ programming skills and embedded system integration capabilities.
  - Achieved high grades for both theoretical (8.7/10) and practical lab (9.5/10) components.

- **Digital Communication System Simulation** *Jan 2024 - Apr 2024*
  Group Project (Course: Digital Communications)
  - Role: Providing theoretical insights for the team, and verification for the results.
  - Analyzed A-Law and μ-Law companding techniques for speech signal processing using MATLAB, evaluating signal-to-quantization noise ratio (SQNR).

- **ZF & MMSE Equalizer Simulation for Wireless Channels** *Sep 2024 - Nov 2024*
  Group Project (Course: Wireless Communications)
  - Role: Analyze, research and give insights on the reasons of performance of different equalization methods.
  - Contributed to the simulation of a QPSK communication system over a frequency-selective AWGN channel using MATLAB by analyzing channel effects.
  - Analyzed the modeled channel using a multi-tap impulse response and its calculated frequency response (FFT).
  - Researched and analyzed the performance of frequency-domain Zero-Forcing (ZF) and Minimum Mean Square Error (MMSE) equalizers used to mitigate Inter-Symbol Interference (ISI).
  - Calculated and compared the Signal-to-Noise Ratio (SNR) before and after applying ZF and MMSE equalization.
  - Analyzed the performance of the equalizers by visualizing the received and equalized signals using constellation diagrams and eye diagrams.

SKILLS

- **Hardware Description Languages:** Verilog HDL
- **FPGA Tools:** Intel Quartus Prime, Platform Designer (Qsys), ModelSim/Questa Sim, Intel FPGAcademy Platform (DE10-Standard), AMD (Xilinx) Vivado
- **Hardware Concepts:** Computer Architecture, Cache Coherence, Memory Consistency, Digital Logic Design, SoC Design & Integration, Hardware Acceleration, RISC-V (Nios V), DMA Controllers, Avalon Bus Interfaces, DCT, Low-Power Design, FPGA (Intel Cyclone V, Xilinx Virtex)
- **Software/Tools:** Systems Programming, Operating Systems Concepts, Simulink, Linux (Bash Shell), Git, Ashling RiscFree™ IDE, Linux Device Drivers (Basic), Android Studio, GNS3, Simplicity Studio, Arduino IDE, Visual Studio Code
- **Hardware Concepts:** Digital Logic Design, Computer Architecture, SoC Design & Integration, Hardware Acceleration, RISC-V (Nios V), DMA Controllers, Avalon Bus Interfaces, DCT, Low-Power Design, FPGA (Intel Cyclone V, Xilinx Virtex)
- **Programming Languages:** C/C++, Python, MATLAB
- **Embedded Systems:** Silicon Labs Gecko, STM32, ESP32, Arduino, Raspberry Pi
- **Communication Protocols:** BLE (Custom Advertising), UART, SPI, I2C, MQTT, OSPF, DHCP
- **Digital & Wireless Communications:** SNR Analysis, Constellation Diagrams, Eye Diagrams
- **Mobile Development:** Android SDK, Activities, Fragments, SQLite, SharedPreferences, RecyclerView, Adapters, ViewPager2, TabLayout, MVC Pattern, DAO Pattern, Singleton Pattern, MPAndroidChart
- **Networking:** Network Design & Simulation (GNS3), Cisco IOS Configuration (Routers, Switches), VLANs, STP, ACLs, NAT/PAT, VPN (Client-to-Site, Site-to-Site), TCP/IP

- **Server Administration:** Windows Server, Active Directory Domain Services (AD DS), DNS, Group Policy Management, File Sharing & Permissions
- **Cloud & IoT Platforms:** AWS EC2, ThingsBoard
- **Machine Learning:** Deep Learning Concepts, Adversarial Attacks (FGSM, PGD), Meta-Learning, Data Structures & Algorithms

Honors and Awards

University of Science, VNUHCM

- **Certificate of Merit for Excellent Achievements in Student Scientific Research** *AY 2022-2023, and 2024-2025*
  Awarded by the Rector
  - For excellent achievements in scientific research.

Long An High School for the Gifted

- **National Round Participant, Vietnam Olympiad in Informatics** *2020 - 2021*
  - Qualified via Provincial Round Third Prize in 2019 for VOI 2020, and Second Prize in 2020 for VOI 2021.
- **Gold Medal, Southern Summer Camp Olympiad in Informatics VI** *2019*
- **ICPC National Round Qualifier (Vietnam Southern Regional)** *2020*

Languages

- **Vietnamese:** Native
- **English:** Proficient
  - IELTS Academic: 7.0 (Dec 2021) [Certificate]
  - Duolingo English Test: 125 (Dec 2025) [Certificate]